TWR-56F8200

User Manual

Rev. 0.00

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Microcontroller Solutions Group

Contents

Revision History

Revision	Date	Changes
0.00	12 Aug 2012	First draft
0.01	26 Feb 2012	Added review feedback

Overview

The MC56F8200 Tower 32-bit MCU Module (TWR-56F8200) is an evaluation, demonstration and development board. The TWR-56F8200 can operate stand-alone or as the main control board in a Tower system with peripheral modules. It can also be used as the main control board with an APMOTOR56F8000E motor control board.

The following list summarizes the features of the TWR-56F8200:

- 32 bit Digital Signal Controller module featuring MC56F82748
- Tower compatible
- Selectable Power sources:
  - USB on 56F8200 card
  - Barrel connector on 56F8200 card
  - Motor control board plug direct to 56F8200 card, no Tower connection, plug Motor control to nine volts
  - Tower elevator board (USB or Barrel on Primary side)
- Filtered power for VDDA and VSSA on the 32-bit MC56F82748DSC
- MC56F82748 DSC (Digital Signal Controller) in an 64 LQFP package
- Optional 8 MHz crystal circuit for the MC56F82748 DSC
- 9 LEDs controlled by the MC56F82748 DSC
- 2 trimport for user to change analog input voltage
- Motor Control Board connector for the APMOTOR56F8000E motor control board
- Auxiliary Signal connector
- Four Thermistors for single ended or differential analog inputs to the MC56F82748 DSC
- CAN transceiver, header, and termination
- Two push buttons for user input or interrupts to the MC56F82748 DSC
- Reset push button for the MC56F82748 DSC
- JTAG header for the MC56F82748 DSC with header to disconnect from OSBDM/OSJTAG
- Headers to connect SCI signals to either USB bridge with CDC(one channel) or elevator board (two channels) or connect one to each
- Expansion via Primary Elevator connector
- MC9S08JM60 (‘JM60) MCU with a 4 MHz crystal provides:
  - Open Source Debug (OSBDM/OSJTAG) circuit
  - USB to SCI bridge with CDC and other techniques supported by third parties
  - Simultaneous OSBDM/OSJTAG and USB to SCI bridge functions with no header required to select
  - Bootloader enable header allows easy upgrade to latest S08 firmware pushed down by CodeWarrior
  - BDM header for the MC9S08JM60 MCU
  - Status and Target Power indicator LEDs

- Control of semiconductor switch to enable power to board from USB
- Voltage translators between 5V MC9S08JM60 MCU chip and 3.3V MC56F82748 DSC chip

1.1 Block Diagram

A block diagram for the TWR-56F8200 is shown in Figure 1 below.

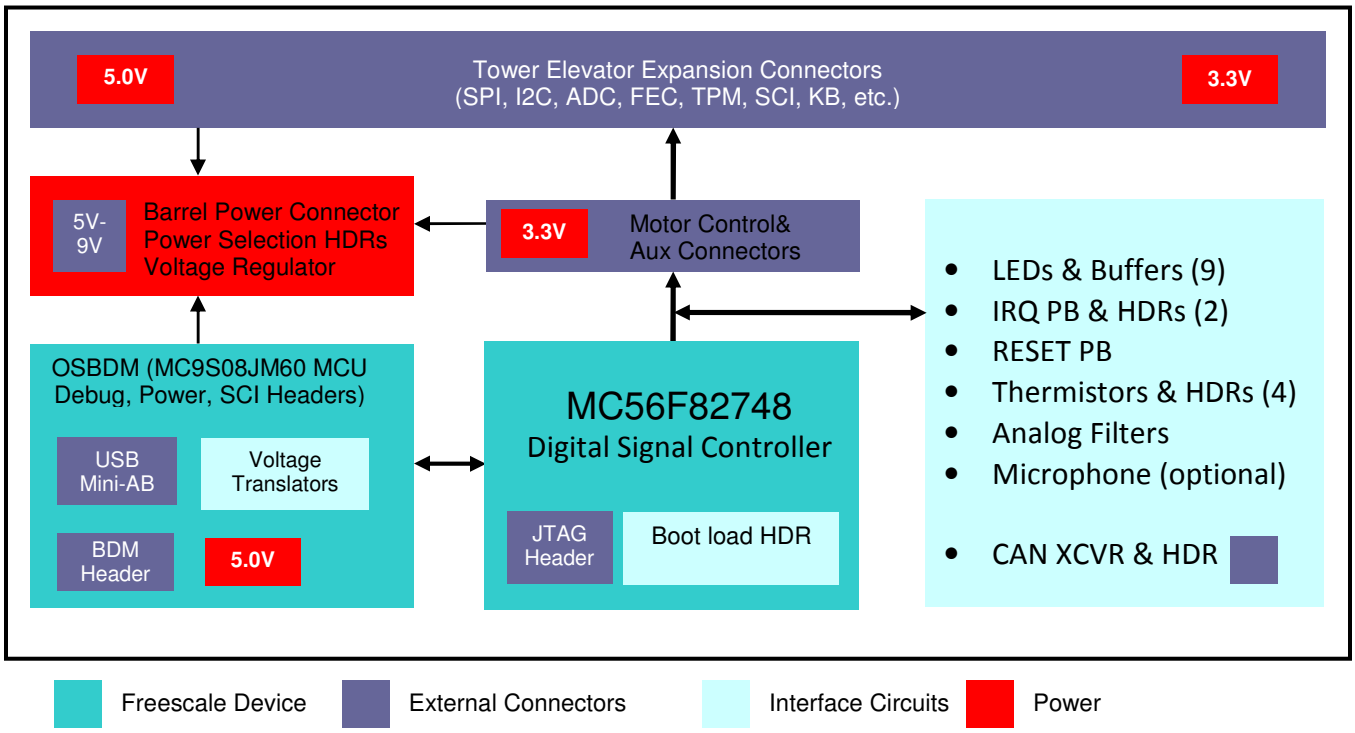


Figure 1. TWR-56F8200 Block Diagram

1.2 Reference Documents

The documents listed below should be referenced for more information on the Freescale Tower system and the TWR-56F8200. Refer to http://www.freesale.com/tower for the latest revision of all Tower documentation.

- *Freescale Tower Electromechanical Specification*
- *TWR-56F8200 Quick Start Guide*
- *TWR-56F8200 Sample code*
- *MC56F82XXX Reference Manual*
- *MC56F82XXX Data Sheet*
- *MC56F82XXX Chip Errata [if exists]*
- *AN3561, USB Bootloader for the MC9S08JM60*
- *APMOTOR56F8000e Motor Control Demonstration System User Manual*

- *AN4413 - BLDC Motor Control with Hall Sensors Driven by DSC using TWR-56F8257 and TWR-MC-LV3PH Boards*

2 Hardware Features

This section provides more details about the features and functionality of the TWR-56F8200.

A drawing of the TWR-56F8200 showing the jack locations is shown in Appendix D. Features are discussed below.

2.1 Tower MCU Module

The TWR-56F8200 board is an MCU Module designed for standalone use (or with a Freescale Tower system) and complies with the electrical and mechanical specification as described in *Freescale Tower Electromechanical Specification*. Connection to the Tower system is through two expansion card-edge connectors that interface to the Elevator boards in a Tower system: the Primary and Secondary Elevator connectors. The Primary Elevator connector, comprised of sides A and B, is utilized by the TWR-56F8200, while the Secondary Elevator connector only makes connections to ground (GND). On sheet 8 of the schematic the J500A and J500B symbols have names assigned to the card edge fingers that correspond with the normal Tower pin assignments.

NOTE: On the top and bottom of one edge of the TWR-56F8200 board, there is a WHITE BELT; the card-edge connectors next to the WHITE BELT on the TWR-56F8200 board should be connected to the Primary Elevator board which uses the WHITE PCI connector. The card-edge connectors without the WHITE BELT on the TWR-56F8200 board should be connected to the secondary Elevator board (or left unconnected) using the Black PCI connector. This instruction over-rides any silkscreen information that may be present, such as the words “Primary” or “Secondary” on the TWR-56F8200, since early revisions had this reversed.

2.2 System Power

The TWR-56F8200 board has three power rails. They are P5V_USB, P3_3V and P3_3V/5V. They are sourced and used as follows:

2.2.1 P5V_USB

The P5V_USB power rail is derived from the Mini-B USB connector at J18 and the inductor at L2. It is used to power the on board OSBDM/OSJTAG/Serial Bridge circuit. This consists of the OSBDM/OSJTAG MCU at U6, several pull-up resistors at R13, R14, R15, R527, and R528, the USB power switch at U501,

and the STATUS and TPWR LEDs at D12 and D13. If there is no USB cable connected to J18 there is no power on this rail and these circuits are all powered down.

2.2.2 P3_3V

The P3_3V power rail is derived from a) the P3_3V_MOTOR power net from the motor control board connector at J501, b) the P3_3V_ELEV power net from the tower connector at J500, or c) the on board 3.3V regulator at U1. The selection of which source is made with a shunt from J7-2 to another pin of J7 or to J6. **Table 6** shows the operation of the different shunt positions. The selection of power into the regulator is made with a shunt from J11-2 to another pin of J11 or to J10 which selects from a) the P5V_TRG_USB power net out of the USB switch at U501, b) the P5V_ELEV power net from the elevator connection at J500 pins A1 and B1, or c) the PWR_IN power net from the 2mm barrel jack at J3 through resettable fuse F1. **Table 6** shows the operation of the different shunt positions. The barrel jack input is protected from reverse voltage inputs by diode D11. The input to the barrel jack may be from a 5V to 9V source and needs to be center positive.

The P3_3V power rail provides power to the majority of the circuits on the board including the MC56F82748 (including the analog power pins through L500 and L501), inverters at U500 and U502, a buffer at U505, the on board LEDs at D1-D9, the thermistor divider circuits at RT1-RT4, and the pull-up resistors at R2, R3, R11, R565, R570, and R562.

2.2.3 P3_3V/5V

The P3_3V/5V power rail is derived from the diode OR (using D500 and D501) of a) the P5V_ELEV power net from the elevator connection (J500 pins A1 and B1), b) the P5V output of the USB power switch at U501, or c) the P3_3V power rail from J7. When there is a USB cable connected or when the tower elevator boards are connected this power rail will be a Schottky diode drop (about 0.3V) below the 5V power nets. When there is no 5V source this power rail will be a Schottky diode drop below the P3.3V power rail. This allows the inputs of the ICs powered by this rail to stay in a high impedance state instead of loading down the inputs through the input protection diodes as would happen if there were no power supplied to the buffers.

2.2.4 Default Power Configuration

The TWR-56F8200 board default power configuration uses the OSBDM/OSJTAG USB port for all power. As soon as the OSBDM/OSJTAG firmware has started it negotiates with the Host PC USB port for full USB power. Once approved it enables the 5V USB power switch (U501) which provides 5V to the P3_3V/5V power rail and to the 3.3V regulator (U1) through headers J10 and J11. Likewise, the on board voltage regulator provides 3.3V to the P3_3V power rail through headers J6 and J7. The 3.3V regulator is able to provide up to 700 mA subject to the power dissipation and temperature limits of the device.

2.3 MC56F82748 DSC

The primary circuits on the board are related to the MC56F82748 DSC. This part is supplied in a surface mounted 64pin LQFP package at U2. Although the board was laid out to allow a ZIF socket at U3 in parallel to the chip at U2 the TWR-56F8200 is only available for purchase with the surface mounted chip.

2.3.1 Clock Sources for the MC56F82748 DSC

Three options are provided for clocking the MC56F82748 device:

1. Oscillator internal to the MC56F82748 chip – approximately 8 MHz.
2. 8 MHz crystal
3. External clock input from Primary Tower Connector or the AUX Connector.

The internal oscillator is used to clock the MC56F82748 immediately following reset. This is the default operation. In this mode the zero ohm resistors at R4 and R10 allow the GPIOC0 and GPIOC1 pins of the MC56F82748 to be used as inputs or outputs.

To use an external crystal with the MC56F82748, zero ohm resistors R4 and R10 must be removed and placed in the R5 and R7 positions. The desired crystal, load capacitors, and parallel resistor (if needed) must be soldered to the board at Y1, C5, C6, and R6. (These components are not provided with the TWR-56F8200 kit.) Following reset, reconfigure the GPIOC0 and GPIOC1 pins to the XTAL and EXTAL functions to allow the use of an external crystal.

To use an external clock for the MC56F82748 make sure the zero ohm resistors are installed at R4 and R10 and removed from R5 and R7. Provide a clock signal on either the Primary Tower Connector J500A - pin B24 (the pin designated as CLOCKIN0) or on the AUX connector J502 - pin 8. Following reset, configure the GPIOC0 pin to the CLKIN input function. In this mode the zero ohm resistor at R10 allows the GPIOC1 pin of the MC56F82748 (pin 10) to be used as an input or output.

2.3.2 Serial I/O Source Select Headers

The TWR-56F8200 board allows the UART functions of the MC56F82748 DSC to be connected to a serial interface at the primary Tower Connector J500A or through a USB bridge to the Host PC using the OSBDM/OSJTAG MCU (U6). The selection of the RXD connections is done with the header at J8 as shown in **Table 1.** The selection of the TXD connections is done with the header at J9 as shown in **Table 2.**

Table 1. J8 – RXD Source Select Header

J8 – RXD Source Select Header		
Pin #	**Connected Signal**	**Description**
1	ELEV_RXD0 at J500A pin A41	Shunt pins 1 and 2 together to connect the DSC

J8 – RXD Source Select Header		
Pin #	**Connected Signal**	**Description**
		RXDO pin to the primary Tower Connector RXD0 pin. (This is a default position.)
2	GPIOF8/RXD0/TB1 from the 56F82748 DSC – pin 6 (RXD0 function)	
3	RXD_SEL from the USB bridge function on the OSBDM/OSJTAG MCU.	Shunt pins 2 and 3 together to connect the DSC RXD0 pin to the USB serial bridge function. Shunt pin 3 and 4 together to connect the DSC RXD1 pin to the USB serial bridge function.
4	GPIOF5/RXD1/XB_OUT5 from the 56F82748 DSC – pin 42 (RXD1 function)	
5	ELEV_RXD1 at J500 pin A43	Shunt pins 4 and 5 together to connect the DSC RXD1 pin to the primary Tower Connector RXD1 pin. (This is a default position.)

Table 2. J9 – TXD Source Select Header

J9 – TXD Source Select Header		
Pin #	**Connected Signal**	**Description**
1	ELEV_TXD0 at J500A pin A42	Shunt pins 1 and 2 together to connect the DSC TXDO pin to the primary Tower Connector TXD0 pin. (This is a default position.)
2	GPIOC2/TXD0/TB0/XB_IN2/CLKO from the 56F82748 DSC – pin 5 (TXD0 function)	
3	TXD_SEL to the USB bridge function on the OSBDM/OSJTAG MCU.	Shunt pins 2 and 3 together to connect the DSC TXD0 pin to the USB serial bridge function. Shunt pin 3 and 4 together to connect the DSC TXD1 pin to the USB serial bridge function.
4	GPIOF4/TXD1/XB_OUT4 from the 56F82748 DSC – pin 41 (TXD1 function)	
5	ELEV_TXD1 at J500 pin A44	Shunt pins 4 and 5 together to connect the DSC TXD1 pin to the primary Tower Connector TXD1 pin. (This is a default position.)

As can be seen in the tables the 56F82748 DSC serial signals may be connected to either the Tower serial signals or to the USB bridge chip; however, only one channel may be connected to the USB bridge chip. If the associated 56F82748 DSC serial pins are not being used for the serial functions the

shunts should be removed from those pins. For more information on the USB Serial Bridge function see section **2.4.2 USB Serial Bridge Interface**.

There are boards available, such as TWR-SER that provide serial ports based on these elevator (ELEV_) connections. These boards can work with the TWR-56F8200 if configured and installed in the same tower system.

2.3.3 LEDs Controlled by the MC56F82748 DSC

There are nine LEDs with buffers connected to the MC56F82748 DSC. Inverting buffers (U500A-F and U502D-F) isolate the LEDs from the DSC pins by providing high impedance inputs. The LEDs are powered by the P3_3V rail and draw about 5mA each. **Table 3** shows the DSC pin names associated with each LED.

Table 3. LEDs Controlled by the MC56F82748 DSC

LEDs Controlled by the MC56F82748 DSC				
MC56F82748 DSC Pin Name	**MC56F82748 Pin Number**	**LED Reference**	**LED Label**	**LED Color**
GPIOE0/PWM0B	45	D1	E0	Green
GPIOE1/PWM0A	46	D2	E1	Yellow
GPIOE2/PWM1B	47	D3	E2	Green
GPIOE3/PWM1A	48	D4	E3	Yellow
GPIOE4/PWM2B/XB_IN2	51	D5	E4	Green
GPIOE5/PWM2A/XB_IN3	52	D6	E5	Yellow
GPIOE6/PWM3B/XB_IN4	53	D7	E6	Green
GPIOE7/PWM3A/XB_IN5	54	D8	E7	Yellow
GPIOF6/TB2/PWM3X	94	D9	F6	Amber

2.3.4 Motor Control Connector

The TWR-56F8200 board may be connected to a motor control board such as the APMOTOR56F8000E. The motor control connector (J501) is on the bottom of the board to provide a convenient connection to the motor control board.

Some of the MC56F82748 DSC pins are connected to the motor control connector. Those pins associated with analog inputs have 100 ohm resistors in series to provide some ESD protection for the analog inputs of the DSC. Those pins providing analog signals from the motor control board have 2200 pf caps with the resistors to provide a low pass filter. The connector pin out is shown in **Table 4**.

Table 4. Motor Control Connector Pin Out

Motor Control Connector J501 Pin Out			
Pin #	**MC56F82748 DSC Signal**	**Pin #**	**MC56F82748 DSC Signal**
1	P3_3V_MOTOR	2	GPIOB7/ANB7&ANC15&CMPB_IN2 (With 100 ohms in series)
3	GND	4	RESETB/ GPIOD4 (With 0 ohms in series – remove to isolate)
5	GPIOF4/TXD1/XB_OUT8	6	GPIOA3/ANA3&VREFLA&CMPA_IN2 (With 100 ohms in series)
7	GPIOF3/SDA1/XB_OUT7	8	GND
9	GPIOE1/PWMA_0A	10	GPIOA0/ANA0&CMPA_IN3/CMPC_O (With 100 ohm, 2200 pf low pass filter)
11	GPIOE0/PWMA_0B	12	GPIOA1/ANA1&CMPA_IN0 (With 100 ohm, 2200 pf low pass filter)
13	GPIOC3/TA0/CMPA_O/RXD0/CLKIN1	14	GPIOA2/ANA2&VREFHA&CMPA_IN1 (With 100 ohm, 2200 pf low pass filter)
15	GPIOC13/TA3/XB_IN6/EWM_OUT_B	16	GND
17	GPIOC4/TA1/CMPB_O/XB_IN8/EWM_OUT_B	18	GPIOB0/ANB0&CMPB_IN3 (With 100 ohm, 2200 pf low pass filter)
19	GPIOC6/TA2/XB_IN3/CMP_REF	20	GPIOB1/ANB1&CMPB_IN0 (With 100 ohm, 2200 pf low pass filter)
21	GPIOC15/SCL0/XB_OUT5	22	GPIOB2/ANB2&VREFHB&CMPC_IN3 (With 100 ohm, 2200 pf low pass filter)
23	GPIOC14/SDA0/XB_OUT4	24	GND
25	TDI /GPIOD0	26	GPIOE7/PWMA_3A/XB_IN5/PWMB_2A
27	TDO/ GPIOD1	28	GPIOE6/PWMA_3B/XB_IN4/PWMB_2B
29	TCK/GPIOD2	30	GPIOE3/PWMA_1A
31	TMS /GPIOD3	32	GPIOE2/PWMA_1B
33	GPIOB3/ANB3&VREFLB&CMPC_IN0 (With 100 ohms in series)	34	GPIOE5/PWMA_2A/XB_IN3
35	GPIOB4/ANB4&ANC12&CMPC_IN1 (With 100 ohms in series)	36	GPIOE4/PWMA_2B/XB_IN2
37	GPIOB5/ANB5&ANC13&CMPC_IN2 (With 100 ohms in series)	38	GPIOA4/ANA4&ANC8&CMPD_IN0 (With 100 ohms in series)
39	GPIOB6/ANB6&ANC14&CMPB_IN1 (With 100 ohms in series)(100K trimport in parallel)	40	GPIOA5/ANA5&ANC9 (With 100 ohms in series)(100K trimport in parallel)

2.3.5 Auxiliary Connectors

In addition to the motor control connector the TWR-56F8200 board also provides two auxiliary connectors J502 on the bottom of the board. These connectors provide access to the MC56F82748 DSC signals that are not covered by the motor control connector. Those pins associated with analog inputs have 100 ohm resistors in series to provide some ESD protection for the analog inputs of the DSC. The connector pin out is shown in **Table 5**.

Table 5. Auxiliary Connector J502 Pin Out

Auxiliary Connectors J502 Pin Out			
Pin #	**MC56F82748 DSC Signal**	**Pin #**	**MC56F82748 DSC Signal**
J502-1	GPIOF0/XB_IN6/TB2/SCK1	J502-2	GPIOA6/ANA6&ANC10 (With 100 ohms in series)
J502-3	GPIOF1/CLKO1/XB_IN7/CMPD_O	J502-4	GPIOA7/ANA7&ANC11 (With 100 ohms in series)
J502-5	GPIOF2/SCL1/XB_OUT6	J502-6	GND
J502-7	GPIOF5/RXD1/XB_OUT9	J502-8	GPIOC0/EXTAL/CLKIN0
J502-9	GPIOF6/TB2/PWMA_3X/PWMB_3X/XB_IN2	J502-10	GPIOC1/XTAL
J502-11	GPIOF7/TB3/CMPC_O/SS1_B/XB_IN3	J502-12	GPIOC2/TXD0/TB0/XB_IN2/CLKO0
J502-13	GPIOF8/RXD0/TB1/CMPD_O	J502-14	GPIOC5/DACO/XB_IN7
J502-15	GPIOC11/CANTX/SCL1/TXD1	J502-16	GPIOC7/SS0_B/TXD0
J502-17	GPIOC12/CANRX/SDA1/RXD1	J502-18	GPIOC8/MISO0/RXD0/XB_IN9
J502-19	GND	J502-20	GPIOC9/SCK0/XB_IN4
J502-21	No Connection	J502-22	GPIOC10/MOSI0/XB_IN5/MISO0
J502-23	No Connection	J502-24	No Connection
J502-25	No Connection	J502-26	No Connection

2.3.6 Tower Elevator Connectors

The TWR-56F8200 board features two expansion card-edge connectors that interface to Elevator boards in a Tower System: the Primary and Secondary Elevator connectors. The Primary Elevator connector, comprised of sides A and B, is utilized by the TWR-56F8200 board, while the Secondary Elevator connector only makes connections to ground (GND). **Table 7** in **Appendix A – Tower Elevator Connector Pin Functions** lists the pin functions for the Primary Elevator Connector.

2.3.7 Thermistors as Analog Inputs

The TWR-56F8200 board provides four thermistors (RT1-4) near the corners of the board that can be used as single ended or differential analog inputs to the MC56F82748 DSC as can be seen on sheet 6 of the schematic. In addition to each thermistor there is a resistor between the thermistor and P3_3V and another resistor between the thermistor and ground. The thermistors are all 10K ohm parts but the associated divider chain uses different resistors. This makes the voltage across the thermistor larger or smaller and provides the ability to try the different gain settings on the analog channels. All four thermistor circuits are designed to provide useable differential inputs over the temperature range of 90˚C to -20˚C. RT2 and RT4 both give a differential voltage of ~1.65V at 25˚C. RT1 gives a differential voltage of 0.10V and RT3 gives a differential voltage of 0.28V at 25˚C.

In addition to the thermistor voltage divider chain each thermistor has a 0.1 uF capacitor in parallel. Each thermistor circuit also has a header that allows the thermistor to be disconnected from the analog inputs to the DSC. If a user wishes to apply an external analog value these headers may be removed and the external analog signal attached to the DSC side of the headers. Finally, each analog input to the DSC has a 100 ohm series resistor and a 2200 pF capacitor as a low pass filter. This helps protect the DSC from electrostatic discharges and lowers the impedance of the analog signal so that it can be sampled with less noise.

2.3.8 CAN Transceiver

The TWR-56F8200 board has a CAN transceiver circuit that may be connected to the CAN pins of the DSC. The CAN transceiver (U503) can be connected to the GPIOC11/CANTX/SCL1/TXD1 and GPIOC12/CANRX/SDA1/RXD1 pins of the DSC through the header at J16. Installing a shunt from pin 1 to pin 2 connects the TXD nets and installing a shunt from pin 3 to pin 4 connects the RXD nets. Note that the GPIOC11/CANTX/SCL1/TXD1 and GPIOC12/CANRX/SDA1/RXD1 nets also go to the primary elevator edge connector (J500A) pins B41 and B42 and to the Auxiliary connector (J502) pins 15 and 17. When using these nets for CAN communications care must be taken that these nets are not driven from these other connectors.

The transceiver is capable of running from 3.3V and is powered by the P3_3V/5V power rail. The transceiver output is connected to header J13 with CANH connected to pin 4 and CANL connected to pin 3. A 120 ohm parallel termination resistor,R560, may be connected between these nets by installing a shunt on header J15.

2.3.9 IRQ or Input Pushbuttons

The TWR-56F8200 board has two pushbuttons (SW1 and SW2) that can be used to provide inputs or interrupts to the DSC. Each has a 10K ohm pull up resistor to P3_3V and a 0.1 uF capacitor to ground to minimize bounce on the output.

Pushbutton SW1 is connected to header J4 where the switch output can be connected to either DSC pin GPIOC2/TXD0/TB0/XB_IN2/CLKO (default) or GPIOF6/TB2/PWM3X depending on the position of the shunt on the header (pin 1 to pin 2 is the default). Similarly, pushbutton SW2 is connected to header J5 where the switch output can be connected to either DSC pin GPIOF8/RXD0/TB1 (default) or GPIOF7/TB3 depending on the position of the shunt on the header (pin 1 to pin 2 is the default).

If the pushbutton switches are not being used as an interrupt, or other purpose, it is best to remove the shunt to the DSC so that the 0.1 uF capacitor is not loading down the DSC pins.

2.3.10 RESET

The GPIOD4/RESET_B pin of the DSC is connected to the motor control connector and the tower connector but also to a pushbutton (SW3) and through buffers to the OSBDM/OSJTAG chip. It is pulled to P3_3V by a 10K ohm resistor. It may be pulled low by the pushbutton or by Q1 in response to a high output from the OSBDM/OSJTAG chip (pin 1) on the TRESET_OUT net. The state of the GPIOD4/RESET_B signal is provided to the OSBDM/OSJTAG chip through a voltage translator (U504B). This buffer is powered by the P3_3V/5V power rail so that its input will remain high impedance when there is no USB cable connected. The buffered RESET signal is provided to pin 33 of the OSBDM/OSJTAG chip and is used by the OSBDM/OSJTAG program in that chip.

2.3.11 JTAG Header and OSBDM/OSJTAG Disconnect Header

The TWR-56F8200 board includes an OSBDM/OSJTAG circuit as a debug interface to the MC56F82748 DSC for normal purposes. If the user desires to use a different debugger connection, header J14 provides a connection point for an external JTAG aware debugger. If an external debugger is connected to the JTAG header the shunts at J21 (pins 1 to 2, 3 to 4, 5 to 6, and 7 to 8) which connect the OSBDM/OSJTAG circuit to the JTAG signals should be removed, allowing the external debugger to control the JTAG port, rather than the ‘JM60.

The TWR-56F8200 board provides a 2.2K ohm pull up resistor to 3.3V on the TMS line. If an external JTAG aware debugger also has a pull up on this line, the external debugger may not be able to pull the TMS line low. If this happens, remove one of the pull up resistors on the TMS line.

2.4 OSBDM/OSJTAG

2.4.1 Debug Interface

An on-board MC9S08JM60 based Open Source BDM (OSBDM/OSJTAG) circuit provides a debug interface to the MC56F82748. A standard USB A male to Mini-B male cable (supplied) can be used for debugging via the USB connector, J18.

2.4.2 USB Serial Bridge Interface

The on-board MC9S08JM60 can also be used as a USB to Serial bridge interface for the UART signals from the MC56F82748 DSC. This bridge circuit is described in detail in section **2.3.2 Serial I/O Source Select Headers.**

The RXD_SEL signal goes to the MC56F82748 DSC. The USB bridge chip is powered by 5V so its output is a 5V output. The buffer (U505) is able to accept the 5V signal from the USB bridge chip (T_TXD1) and converts it to the 3.3V signal (RXD_SEL) for the DSC. The buffer output is enabled by an inverted RTS signal (TXD_RXD_EN_B) from the USB bridge chip. If there is no USB connection to the TWR board the RTS signal is not driven and the 3.3V powered inverter (U502C) input is biased low disabling the output of the buffer.

In a similar way TXD_SEL is a 3.3V signal from the MC56F82748 DSC. The USB bridge chip is expecting a 5V input on T_RXD1. The buffer between these two signals (U504C) is powered by P3_3V/5V. It will accept the 3.3V input from the DSC and convert it to the 5V signal needed by the USB bridge chip. The buffer output is enabled by the same inverted RTS signal (TXD_RXD_EN_B) discussed above. If there is no USB connection to the TWR board, the RTS signal is not driven and the 5V powered buffer disabled so nothing is driving the powered down USB bridge chip.

The serial interface signals from the MC56F82748 DSC may be routed to the MC9S08JM60 serial interface via header and Berg straps. Using the USB serial bridge the MC9S08JM60 will convert the serial interface data into USB packets and send them to the host PC where they may be handled by a PC application normally conversant with a serial port.

2.4.3 Clocking the OSBDM/OSJTAG MCU (MC9S08JM60)

The MC9S08JM60 MCU uses an on board 4 MHz external crystal circuit (Y2, R16, C7, and C9) for its clock. There are no user options for clocking the MC9S08JM60.

2.4.4 Reserved Function Select Header

Header J20 selects whether the on-board MC9S08JM60 MCU operates as an OSBDM/OSJTAG debug interface or as a USB Serial Bridge interface on *older* versions of S08 firmware such as may have existed

on prototypes of the TWR56F8200. Leaving the shunt on the header enables the OSBDM/OSJTAG debug interface. Removing the shunt on header J20 enables the USB Serial Bridge interface. The header, J20, is subsequently reserved for future use.

2.4.5 Bootloader Enable

In addition to the OSBDM/OSJTAG Debug interface and the USB Serial Bridge interface the MC9S08JM60 device used in the OSBDM/OSJTAG circuit is preprogrammed with a USB Bootloader. The USB Bootloader will run following a power-on reset if a shunt is installed on header J17. This allows in-circuit reprogramming of the JM60 flash memory via USB. This enables the OSBDM/OSJTAG firmware to be upgraded by the user when upgrades become available. In normal OSBDM/OSJTAG / USB Serial Bridge operation this shunt must be left off. For details on the USB Bootloader, refer to Application Note AN3561 on the Freescale website (http://www.freescale.com
The USB Bootloader communicates with a GUI application running on a host PC. The GUI application can be found on the Freescale website; search keyword "JM60 GUI". Refer to section 2.5 and 3.3 of AN3561 for details on installing and running the application.

2.4.6 BDM Header

The BDM header at J22 is used for initial programming of the MC9S08JM60 MCU or if reprogramming when the bootloader fails. An external 9S08 BDM debugger would be connected to J22 and used to program the MCU. This is not expected to be a normal user interface, however it is useful if the 'JM60 device is inadvertently reprogrammed with firmware that is not functional.

2.4.7 OSBDM/OSJTAG Status LEDs

The MC9S08JM60 OSBDM/OSJTAG MCU controls two status LEDs at D12 and D13. Refer to the OSBDM/OSJTAG instructions for the meaning of the LEDs.

2.4.8 OSBDM/OSJTAG Voltage Translation

Since the OSBDM/OSJTAG MCU runs from 5V and the 56F82748 DSC runs from 3.3V there needs to be voltage translation between the two circuits. This is done through U505, U504A and U502B. U505 has 5V tolerant inputs and provides 3.3V signals (TCK, TDI, and TMS) to the DSC's JTAG pins through the shunts on header J21. U504A is powered by the P3_3V/5V rail and translates the 3.3V TDO signal from the DSC to a 5V signal for the OSBDM/OSJTAG MCU. The outputs of both of these translators are high impedance if the signal OUT_EN_B goes high. This happens if the OSBDM/OSJTAG circuit looses power (no power to the USB connector). In that case the OUT_EN signal from the OSBDM/OSJTAG MCU (pin 15) is biased low by R12. The inverter at U502B then drives OUT_EN_B high in response. Additional information is included in section **2.4.2**.

3 Jumper Table

There are several headers provided for isolation, configuration, and feature selection. Refer to **Table 6** for details. The default shunt positions are shown in **bold**.

Table 6. TWR-56F8200 Jumper Table

Jumper	Function	Shunts	Description	Use Case
J1	Thermistor RT1 Connect	**1-2, 3-4**	**Connect RT1 circuit to the MC56F82748 DSC**	
		none	Disconnect RT1 circuit from the MC56F82748 DSC	
J2	Thermistor RT2 Connect	**1-2, 3-4**	**Connect RT2 circuit to the MC56F82748 DSC**	
		none	Disconnect RT2 circuit from the MC56F82748 DSC	
J4	IRQ1 Select	**1-2**	**Connect SW1 to MC56F82748 DSC pin GPIOC2/TXD0/TB0/XB_IN2/CLKO**	
		2-3	Connect SW1 to MC56F82748 DSC pin GPIOF6/TB2/PWM3X	
		none	Disconnect SW1 from the MC56F82748 DSC	
J5	IRQ0 Select	**1-2**	**Connect SW2 to MC56F82748 DSC pin GPIOF8/RXD0/TB1**	
		2-3	Connect SW2 to MC56F82748 DSC pin GPIOF7/TB3	
		none	Disconnect SW2 from the MC56F82748 DSC	
J6 and J7	3.3V Source Select	**J6-1 to J7-2**	**Connect the on-board voltage regulator to the P3_3V power rail**	**1,2,3a**
		J7-1 to J7-2	Connect P3_3V_MOTOR to the P3_3V power rail (power the 3.3V rail from the motor control connector)	4
		J7-2 to J7-3	Connect P3_3V_ELEV to the P3_3V power rail (power the 3.3V rail from the tower connector)	3
		J7-2 open	Disconnect the P3_3V power rail – no power	
J8	RXD Source Select (note that only one connection can be made to pin 3 at a time)	**1-2**	**Connect ELEV_RXD0 from the Tower connector to MC56F82748 DSC pin GPIOF8/RXD0/TB1**	
		2-3	Connect RXD_SEL from the USB Serial Bridge to MC56F82748 DSC pin **GPIOF8/RXD0/TB1**	
		Pin 2 open	Disconnect MC56F82748 DSC pin **GPIOF8/RXD0/TB1**	
		3-4	Connect RXD_SEL from the USB Serial Bridge to MC56F82748 DSC pin GPIOF5/RXD1/XB_OUT5	
		4-5	**Connect ELEV_RXD1 from the Tower connector to MC56F82748 DSC pin GPIOF5/RXD1/XB_OUT5**	
		Pin 4 open	Disconnect MC56F82748 DSC pin GPIOF5/RXD1/XB_OUT5	

Jumper	Function	Shunts	Description	Use Case
J9	TXD Source Select (note that only one connection can be made to pin 3 at a time)	**1-2**	**Connect ELEV_TXD0 from the Tower connector to MC56F82748 DSC pin GPIOC2/TXD0/TB0/XB_IN2/CLKO**	
		2-3	Connect TXD_SEL from the USB Serial Bridge to MC56F82748 DSC pin GPIOC2/TXD0/TB0/XB_IN2/CLKO	
		Pin 2 open	Disconnect MC56F82748 DSC pin GPIOC2/TXD0/TB0/XB_IN2/CLKO	
		3-4	Connect TXD_SEL from the USB Serial Bridge to MC56F82748 DSC pin GPIOF4/TXD1/XB_OUT4	
		4-5	**Connect ELEV_TXD1 from the Tower connector to MC56F82748 DSC pin GPIOF4/TXD1/XB_OUT4**	
		Pin 4 open	Disconnect MC56F82748 DSC pin GPIOF4/TXD1/XB_OUT4	
J10 and J11	5V Source Select	J10-1 to J11-2	Connect the power in barrel connector (through fuse F1) to the input of the 3.3V voltage regulator	1
		J11-1 to J11-2	**Connect P5V_TRG_USB (the switched USB 5V) to the input of the 3.3V voltage regulator**	**2**
		J11-2 to J11-3	Connect P5V_ELEV to the input of the 3.3V voltage regulator	3a
		J11-2 open	Disconnect the input of the 3.3V voltage regulator	3,4
J12	Unused	**open**	**Unused**	
J15	CAN Termination Enable	**1-2**	**Connect the 120 ohm CAN termination resistor**	
		open	No CAN termination	
J16	CAN Enable	**1-2, 3-4**	**Connect the CAN transceiver TXD and RXD to MC56F82748 DSC pins GPIOC11/CANTX/SCL1/TXD1 GPIOC12/CANRX/SDA1/RXD1**	
		open	Disconnect the CAN transceiver	
J17	MC9S08JM60 Bootload Enable	1-2	Enable USB bootloading of the MCU Flash memory	
		open	**Disable bootloading**	
J19	Thermistor RT3 Connect	**1-2, 3-4**	**Connect RT3 circuit to the MC56F827 DSC**	
		none	Disconnect RT3 circuit from the MC56F82748 DSC	
J20	RESERVEC / OSBDM/OSJTAG Enable	**1-2**	**Reserved-deprecated**	
		none	Reserved-deprecated	
J21	OSBDM/OSJTAG Connect to JTAG	**1-2, 3-4, 5-6, 7-8**	**Connect the OSBDM/OSJTAG debug signals (JTAG) to the MC56F82748 DSC JTAG pins**	
		none	Disconnect OSBDM/OSJTAG from the MC56F82748 DSC	
J23	Thermistor RT4 Connect	**1-2, 3-4**	**Connect RT4 circuit to the MC56F827 DSC**	
		none	Disconnect RT4 circuit from the MC56F82748 DSC	

Due to the large number of use cases for the TWR-56F8200 board, the Power Use Cases below are in the table above to ease the configuration of the board with Berg Straps and/or wires for power configurations.

The use cases enumerated are:

1. TWR-56F8200 standalone with the barrel power connector and the U-MULTILINK or USB-TAP. Use this mode for initial programming of the board, especially prior to using it to control high voltages.
2. TWR-56F8200 standalone with the USB connector. Use this for OSJTAG programming of the board. No other hardware is required than the board and cable supplied for connection to USB of computer.
3. TWR-56F8200 in Tower system driving TWR-MC-LV3PH board, also in Tower system, or for any other Tower application other than APMOTOR56800E motor driving in tower. (3a is alternative connection.)
4. TWR-56F8200 in Tower system driving APMOTOR56800E (equipped with three 1 inch #4 hardware plastic standoffs (female both ends) with six #4 screws).
5. TWR-56F8200 driving APMOTOR56800E outside the tower system. (Same power configuration as 4).

Appendix A – Tower Elevator Connector Pin Functions

Table 7 provides the pin out for the Primary Elevator Connector. An "**X**" in the "Used" column indicates that there is a connection from the TWR-56F8200 board to that pin on the Elevator connector. An "**X**" in the "Jmp" column indicates that a jumper is available that can isolate the onboard circuitry from the Elevator connector.

The function listed in the "Usage" column is the function(s) that the pin is expected to be programmed to provide when used with the Tower system. All of the MC56F82748 pins (except power) have multiple functions. Not all of the possible functions are shown.

Note that all analog pins (ANAn or ANBn) have a low pass filter to ground consisting of a 100 ohm resistor and a 2200 pf capacitor. This is to protect the analog inputs of the DSC from a static discharge at one of the connectors. See schematic sheets 6 and 7 in
Appendix B – TWR-56F8200 Board Schematic.

Table 7. TWR-56F8200 Primary Elevator Connector Pin Out

TWR-56F8200 Primary Connector									
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B1	**5V_1**	**5V Power**	**X**	**X**	A1	**5V_2**	**5V Power**	**X**	**X**
B2	**GND**	**Ground**	**X**		A2	**GND_9**	**Ground**	**X**	
B3	**3.3V_1**	**3.3V Power**	**X**	**X**	A3	**3.3V_4**	**3.3V Power**	**X**	**X**
B4	ELE_PS_SENSE_1	**(must not be connected)**	**X**	**X**	A4	**3.3V_5**	**3.3V Power**	**X**	**X**
B5	**GND_2**	**Ground**	**X**		A5	**GND_10**	**Ground**	**X**	
B6	**GND_3**	**Ground**	**X**		A6	**GND_11**	**Ground**	**X**	
B7	SDHC_CLK / SPI1_CLK	SCK (see also pin B48)	**X**		A7	I2C0_SCL	SCL0	**X**	
B8	SDHC_D3 / SPI1_CS1_b				A8	I2C0_SDA	SDA0	**X**	
B9	SDHC_D3 / SPI1_CS0_b	SS_B (see also pin B46)	**X**		A9	GPIO9/UART1_CTS1	GPIOA4/ANA4	**X**	X
B10	SDHC_CMD / SPI1_MOSI	MOSI (see also pin B45)	**X**		A10	GPIO8/SDHC_D2	GPIOA5/ANA5	**X**	X
B11	SDHC_D0 / SPI1_MISO	MISO (see also pin B44)	**X**		A11	GPIO7 / SD_WP_DET	GPIOA6/ANA6	**X**	X
B12	ETH_COL_1				A12	ETH_CRS			
B13	ETH_RXER_1				A13	ETH_MDC_1			
B14	ETH_TXCLK_1				A14	ETH_MDIO_1			
B15	ETH_TXEN_1				A15	ETH_RXCLK_1			
B16	ETH_TXER				A16	ETH_RXDV_1			
B17	ETH_TXD3				A17	ETH_RXD3			
B18	ETH_TXD2				A18	ETH_RXD2			
B19	ETH_TXD1_1				A19	ETH_RXD1_1			
B20	ETH_TXD0_1				A20	ETH_RXD0_1			
B21	GPIO1 / UART1_RTS1	GPIOB4/ANB4&CMPC_M1	**X**	X	A21	I2S0_MCLK			
B22	GPIO2 / SDHC_D1	GPIOB5/ANB5&CMPC_M2	**X**	X	A22	I2S0_DOUT_SCLK			
B23	GPIO3	GPIOB6/ANB6&CMPB_M1	**X**	X	A23	I2S0_DOUT_WS			

TWR-56F8200 Primary Connector									
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B24	CLKIN0	XTAL&CLKIN	X	X	A24	I2S0_DOUT_DIN0			
B25	CLKOUT1				A25	I2S0_DOUT_DOUT0			
B26	**GND_4**	**Ground**	X		A26	**GND_12**	**Ground**	X	
B27	AN7	ANB3&CMPC_M0	X		A27	AN3	ANA3&CMPA_M2	X	X
B28	AN6	ANB2&CMPC_P2	X		A28	AN2	ANA2&CMPA_M1	X	
B29	AN5	ANB1&VERFLB&CMPB_M0	X		A29	AN1	ANA1&VREFLA&CMPA_M0	X	
B30	AN4	ANB0&VERFHB&CMPB_P2	X		A30	AN0	ANA0&VREFHA&CMPA_P2/CMPC_O	X	
B31	**GND_5**	**Ground**	X		A31	**GND_13**	**Ground**	X	
B32	DAC1				A32	DAC0	DAC0	X	
B33	TMR3	TA3	X		A33	TMR1	TA1	X	
B34	TMR2	TA2	X		A34	TMR0	TA0	X	
B35	GPIO4	GPIOB7/ANB7&CMPB_M2	X	X	A35	GPIO6	GPIOA7/ANA7	X	X
B36	**3.3V_2**	**3.3V Power**	X	X	A36	**3.3V_6**	**3.3V Power**	X	X
B37	PWM7	PWM3B	X		A37	PWM3	PWM1B	X	
B38	PWM6	PWM3A	X		A38	PWM2	PWM1A	X	
B39	PWM5	PWM2B	X		A39	PWM1	PWM0B	X	
B40	PWM4	PWM2A	X		A40	PWM0	PWM0A	X	
B41	CAN0_RX0	CANRX	X	X	A41	UART0_RX	ELEV_RXD0 (see also pin B61)	X	X
B42	CAN0_TX0	CANTX	X	X	A42	UART0_TX	ELEV_TXD0 (see also pin B62)	X	X
B43	1WIRE				A43	UART1_RX	ELEV_RXD1	X	X
B44	SPI0_MISO/IO1	MISO (see also pin B11)	X		A44	UART1_TX	ELEV_TXD1	X	X
B45	SPI0_MOSI/IO0	MOSI (see also pin B10)	X		A45	VSSA			
B46	SPI0_CS0_b	SS_B (see also pin B9)	X		A46	VDDA			
B47	SPI0_CS1_b				A47	CAN1_RX			
B48	SPI0_CLK	SCK (see also pin B7)	X		A48	CAN1_TX			
B49	**GND_6**	**Ground**	X		A49	**GND_14**	**Ground**	X	
B50	I1C1_SCL1	SCL1	X		A50	GPIO14			
B51	I2C1_SDA1	SDA1	X		A51	GPIO15			
B52	GPIO5/SPI0_HOLD/IO3	GPIOF0	X		A52	GPIO16/SPI0_WP/IO2			
B53	RSRV_B53				A53	GPIO17			
B54	RSRV_B54				A54	USB0_DM			
B55	IRQ_H				A55	USB0_DP			
B56	IRQ_G				A56	USB0_ID			
B57	IRQ_F				A57	USB0_VBUS			
B58	IRQ_E				A58	I2S0_DIN_SCK	TB3	X	X
B59	IRQ_D				A59	I2S0_DIN_WS	TB2	X	X
B60	IRQ_C				A60	I2S0_DIN1			
B61	IRQ_B	TB1 (see also pin A41)	X	X	A61	I2S0_DOUT1			
B62	IRQ_A	TB0 (see also pin A42)	X	X	A62	RSTIN_b	RESET_B	X	
B63	EBI_ALE / EBI_CS1_b				A63	RSTOUT_b	RESET_B	X	
B64	EBI_CS0_b				A64	CLKOUT0	CLKO	X	
B65	**GND_7**	**Ground**	X		A65	**GND_15**	**Ground**	X	
B66	EBI_AD15				A66	EBI_AD14			
B67	EBI_AD16				A67	EBI_AD13			

TWR-56F8200 Primary Connector									
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B68	EBI_AD17				A68	EBI_AD12			
B69	EBI_AD18				A69	EBI_AD11			
B70	EBI_AD19				A70	EBI_AD10			
B71	EBI_R/ W_b				A71	EBI_AD9			
B72	EBI_OE_b				A72	EBI_AD8			
B73	EBI_D7				A73	EBI_AD7			
B74	EBI_D6				A74	EBI_AD6			
B75	EBI_D5				A75	EBI_AD5			
B76	EBI_D4				A76	EBI_AD4			
B77	EBI_D3				A77	EBI_AD3			
B78	EBI_D2				A78	EBI_AD2			
B79	EBI_D1				A79	EBI_AD1			
B80	EBI_D0				A80	EBI_AD0			
B81	**GND_8**	**Ground**	**X**		A81	**GND_16**	**Ground**	**X**	
B82	**3.3V_3**	**3.3V Power**	**X**	**X**	A82	**3.3V_7**	**3.3V Power**	**X**	**X**

Appendix B – TWR-56F8200 Board Schematic

The Schematic supplied as an embedded PDF file. Right click on the cover page below and select Acrobat Document Object, then Open.
Some prototype boards, built with sockets (and they can be so identified.

Adobe Acrobat Document

Appendix C – TWR-56F8200 Board BOM

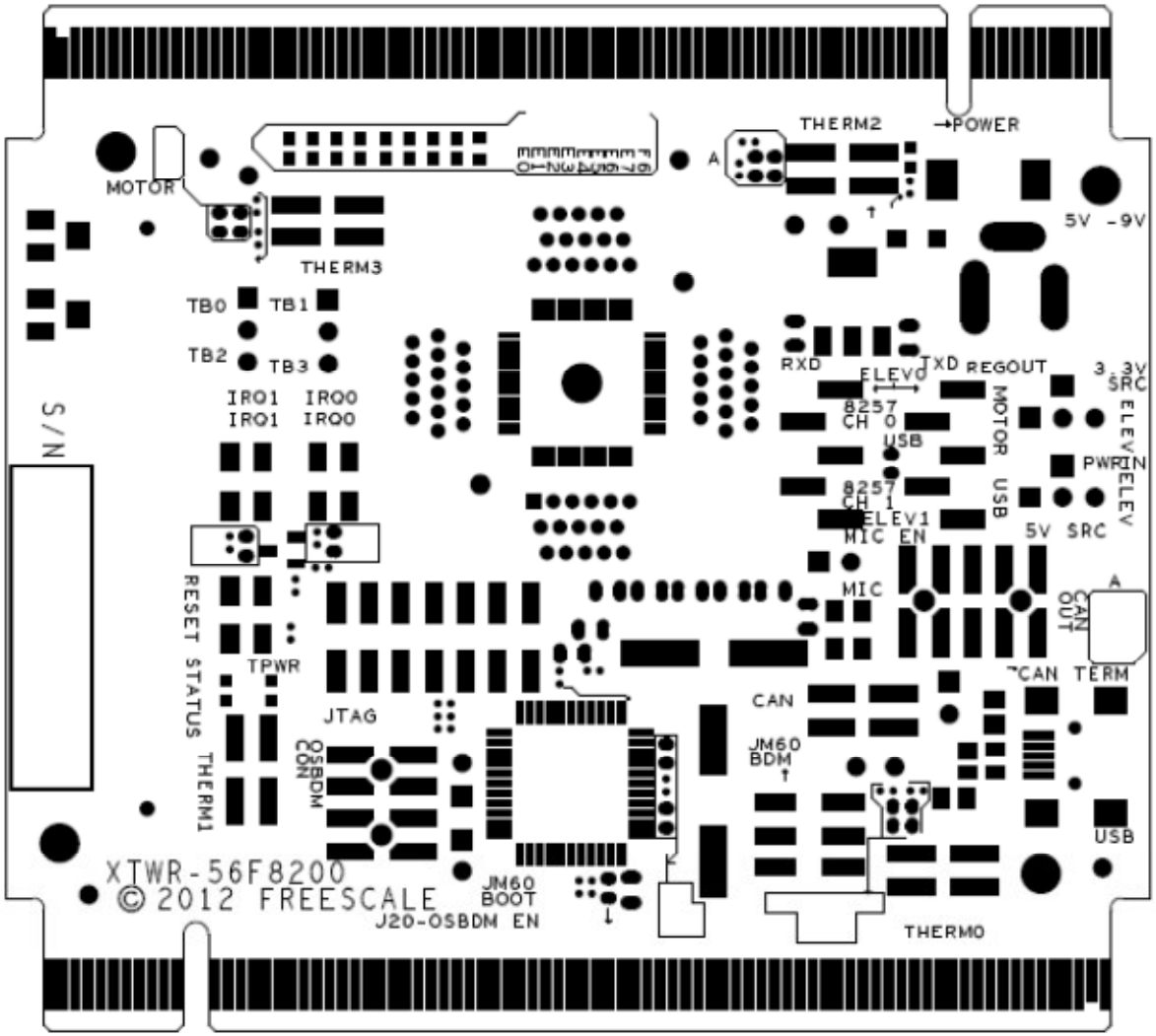
The BOM is supplied as an embedded worksheet object, just below. Right click on the object below and select “Worksheet Object”, then “Open” to read the BOM or work with it as a spreadsheet.

Microsoft Office
Excel Worksheet

freescale™
semiconductor

Freescale Semiconductor Inc.
Microcontroller Solutions Group

Appendix D – TWR-56F8200 Board Jack Layout Top View



Appendix E – TWR-56F8200 Board Jack Layout Bottom View